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RECENT TRENDS IN PARTS SEU (SINGLE EVENT UPSET)

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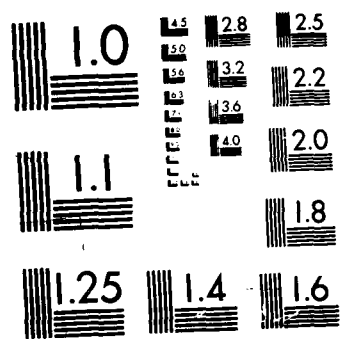
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Recent Trends in Parts SEU Susceptibility from Heavy Ions

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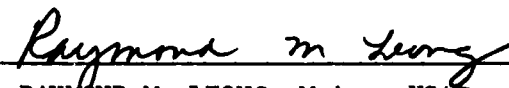
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This report has been reviewed by the Public Affairs Office (PAS) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

This technical report has been reviewed and is approved for publication. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.



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PREFACE

At JPL, special thanks are due to Jim Coss, SEU group leader; the members of the beam team, Carl Malone, George Soli, and Mark Huebner; the device test engineers, Harvey Schwartz, Kevin Watson, and Peter Wang; and the able logistics and trouble-shooting efforts of Mike Havener. The Aerospace authors would like to thank Jon Osborn for producing fast RAM and microprocessor testers, and John Elder for writing extensive software to exercise the test devices, as well as for providing generous help in the analysis of the test results. Thanks are also due to Mike Marra and Bob Walter of Aerospace for constantly updating the experimental hardware and transporting it in good condition to the test site.

Special thanks are due to Ruthmary Larimer and the rest of the staff at the LBL 88-inch cyclotron and to Peter Thieberger and his staff at Brookhaven National Laboratories.

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I. INTRODUCTION

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→ An ongoing single event upset (SEU) program at JPL and the Aerospace Corporation is continuing in order to assess specific parts performance in interplanetary and satellite environments and to establish trends in SEU response of many parts types.

In 1985, Nichols et al (Ref. 1) published a nearly comprehensive listing of SEU test data for 186 parts. This large collection was sufficient to permit generalizations about the parts SEU susceptibility according to their technology, function, and manufacturer.

In this report generalizations are extended to newer classes of parts and the statistical base for some of the previous parts classifications is expanded.

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II. ORGANIZATION AND SCOPE OF DATA

This report presents soft error and latchup experimental test data from the Jet Propulsion Laboratory (JPL) and the Aerospace Corporation during the period from May 1985 through December 1986. However, data taken for the CRRES satellite ground test program,* and proprietary data taken by DNA subcontractors and others is excluded from this survey. Much smaller data sets have been generated by other U.S. and foreign researchers; these data have not been sought for inclusion in this compilation. The data presented here, nevertheless, represent a substantial majority of all test data obtained throughout the world during this period.

The data from JPL and the Aerospace Corporation are presented in two different groups, and there are minor differences in the format of each organization. JPL defines the threshold LET as that value of LET where soft errors are first counted at fluences of approximately 10^6 ions/cm². Aerospace defines this threshold as occurring at that LET where the measured upset cross section is 10% of the measured maximum cross section. These two values may be very different. To obtain SEU rates for a prescribed radiation environment, one requires a plot of cross section vs. LET, provided by the parent test organization.

The JPL data are conveniently divided into two tables; Table 1 for MOS devices and Table 2 for bipolar devices. The Aerospace data are given in Table 3 for all technologies. All data listed here represent a substantial abbreviation and ignore statistical features altogether. Hence, a system designer interested in a specific part is urged to contact the appropriate test organization for further information.

*Data for the CRRES spacecraft program are stored at JPL, with most of the data presently available to the public.

A. TRENDS

1. JPL DATA

Several interesting trends emerge from this set of data. We see (as indicated before in Ref. 1) that the CMOS RAMs have a varying susceptibility to soft errors as demonstrated by the wide variation in threshold LET; the single bipolar RAM reported here is very soft, as expected. Of special note is the fact that an epi-CMOS part exhibited latchup, reported in Ref. 2.

The single test of a PMOS technology register shows that it has a significantly higher threshold LET than the NMOS devices (DRAMs). However, more testing of PMOS technology is required to establish whether PMOS technology is harder than NMOS technology in general.

The NMOS DRAMs are very susceptible to heavy ion upset and much more susceptible than the 4k KMOS DRAM (MCM6605A) reported earlier (Ref. 1) for which the threshold LET was 14 MeV/mg/cm^2 . One can assume that the high density (large number of bits) for the recently tested parts is relevant. It is also noted that the cross sections for the 256k DRAM can exceed the geometrical area of the sensitive regions. This observation strongly implies that multiple upsets can occur in these devices for a single ion strike. The DRAMs are so sensitive, in fact, that a test with protons or neutrons is recommended to assess their SEU response for avionics, as well as low earth orbit and space applications.

Several PROMS were tested during this period and the data support the expectation that transient upset pulses can occur in PROMs for the heavier ions. Unfortunately, the upset threshold LET was not determined in any of these tests. Note also that latchup was observed in one of the bulk CMOS PROMs at an LET of 14 MeV/mg/cm^2 .

All of the CMOS microprocessors are very soft except for the Harris 80C85 which is an equivalent to a specially hardened microprocessor of the Sandia 3000 series.

Four low power TTL bipolar logic devices were tested, which exhibited good resistance to single event upsets. Noteworthy is the fact that two older

(1974) versions of the 54L93 counter and the 54K73 flip-flop were softer than their newer (1982) equivalents, fabricated by the same manufacturer. This result contrasts with the normal trend where newer equivalent devices are usually more SEU susceptible.

For the first time, data is available on some analog-to-digital (A/D) and digital-to-analog (D/A) converter parts. This limited data subset suggests that A/D converters are more SEU susceptible than the D/A converters.

2. AEROSPACE DATA

The Aerospace data show that two NMOS RAMs, a TTL RAM, and an advanced CMOS technology RAM are all very susceptible to soft errors. The data show that CMOS/SOS and CMOS/epi devices are much harder, as expected.

Preliminary results for a large collection of logic devices show 54AHCTXXX devices are hard whereas 54ASXXX technology is fairly soft. The latter technology resembles the response for 54ALSXXX devices reported earlier (Ref. 1).

III. CONCLUSIONS

The new data presented here, when combined with earlier published data, (Ref. 1) list key SEU device response parameters for some 240 device types. That data base permits many useful generalizations and trends to be established. The data can be used to eliminate unacceptable device technologies and to identify for systems those key parts that are expected to be most SEU susceptible.

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1. D. K. Nichols, W. E. Price, W. A. Kolasinski, R. Koga, J. C. Pickel, J. T. Blandford, A. E. Waskiewicz, "Trends in Parts Susceptibility to Single Event Upset from Heavy Ions," IEEE Trans. on Nuc. Sci., NS-32, No. 6, 4189 (Dec. 1985).
2. K. K. Nichols, W. E. Price, M. A. Shoga, J. R. Duffey, W. A. Kolasinski, R. Koga, "Discovery of Heavy-ion Induced Latchup in CMOS/epi Devices," IEEE Trans. on Nuc. Sci., NS-33, No. 6, 1696 (Dec. 1986).

Table 1. Recent JPL SEU Data (MOS Devices)

Device	Function	Technology	Mfr.	Bits	Threshold** Device Cross*** Cross Section			Facility****	Remarks
					LET (MeV/mg/cm ²)	Section (cm ²) (Kr or Br)	Per Bit (10 ⁻⁸ cm ²)		
HC6167R	RAM	CMOS/RESISTOR	Honeywell	16K	>120	-	-	BML	No Latchup (435 Mohm feedback resistor)
MM6516	RAM	CMOS/EPI(%)	Harris	16K	<29	5×10^{-2}	300	UCB-88 1a, BML	Six out of 11 parts latched up with Kr, Br at $\phi > 0$
MM 6516	RAM	CMOS	Harris	16K	<17	-	-	UCB-88 1a	Latches up with Ar and Kr
V1608	RAM	CMOS	VTC	16K	15	2×10^{-2}	120	BML	
MM65262 RH	RAM	CMOS/EPI	Harris	16K	20	10^{-2}	60	UCB-88 1a	
IDT 6116	RAM	NMOS/EPI	IDT	16K	3	7.2×10^{-2}	600	BML	
AM92L44	RAM	NMOS	AMD	4K	1.6	0.41	10 ⁴	ORSAV	
AM21L47	RAM	NMOS	AMD	4K	<1.6	0.41	10 ⁴	ORSAV	
AM2813	FIPO REG.	PMOS	AMD	288	10	6×10^{-3}	2000	UCB-88 1a	
MT1256	DRAM (2CL)	NMOS	Micron Tech	393K	<2	10^{-2}	N/A	BML	ECL logic reduces upset rate
MT1257	DRAM	NMOS	Micron Tech	256K	<2	0.6	240	BML	
M41256	DRAM	NMOS	ATT	256K	<2	0.5	200	BML	
MM1256	DRAM	NMOS	Pujieu	256K	2	0.1	40	BML	
2864	2APROM	NMOS	Intel	64K	<37	10^{-4}	-	UCB-88 1a	
2764A	PRAM	NMOS	Intel	64K	<17	1.5×10^{-3}	-	BML	
27C64	PRAM	CMOS	Intel	64K	-	-	-	BML	Latchup threshold = 16 MeV/mg/cm ²
MM6616	PRAM	CMOS	Harris	2K	<37	10^{-2}	-	UCB-88 1a	
CD16007	Gate Array	CMOS	Lockheed	-	>75	No upset	-	ORSAV	

** LET is Linear Energy Transfer or dE/dx. Threshold is the condition for no upsets for fluences $\geq 10^6$ ions/cm².

*** The cross section (upsets/fluence) is given for 120-300 MeV krypton or bromine ions at normal incidence, having an LET = 39 MeV/(mg/cm²).

**** BML is Brookhaven National Laboratory, UCB-88 1a. is a cyclotron at Lawrence Berkeley Laboratories, Orsay is a new shut-down cyclotron at the Institut de Physique Nucleaire, Orsay, France.

This is a much tested part, having several different epi versions, discussed in another paper in this journal. Some thinner epi versions, tested later, are immune to latchup.

Table 1. Recent JPL SEU Data (MOS Devices) (continued)

Device	Function	Technology	Mfr.	Wits	Threshold**		Facility***	Remarks
					LET (MeV/mg/cm ²)	Device Cross Section (cm ²) (Kr or Br)		
8085	Microprocessor	NMOS	Intel	126/256	<2.8	4×10^{-3}	UCB-88 in	Extrapolated Cross Section
MS32016	Microprocessor	NMOS	MSC	>368	<3	2×10^{-2}	UCB-88 in	Extrapolated Cross Section
MS32081	Float Pt. Unit	NMOS	MSC	>256	<3	6×10^{-3}	UCB-88 in	8 32-bit registers were tested
MS32201	Timing Control	Bipolar*	MSC	>2	6	$> 3 \times 10^{-4}$	UCB-88 in	Only Div 2 and reset #/V tested
32C016	Microprocessor	CMOS	MSC	>368	3	-	BWL	Commercial Mask "C" Latches up with 16 MeV boron (LET = 3 MeV/mg/cm ²)
80C85	Microprocessor	CMOS	Harris	93	>75	No upset	BWL	Equivalent to Samsa SA3000
80C86	Microprocessor	CMOS/EPL	Intel	600	<<12	4×10^{-3}	BWL	Partial characterization
ADSP-1016A	Multiplier	CMOS	AD	-	<37	-	UCB-88 in	Latchup with Kr at 0 degrees

* This bipolar device is included as part of MS32016 peripherals

** LET is Linear Energy Transfer or dE/dx. Threshold is the condition for no upsets for fluences $< 10^6$ ions/cm².

*** The cross section (upsets/fluence) is given for 170-300 MeV krypton or bromine ions at normal incidence, having an LET = 39 MeV/(mg/cm²).

**** BWL is Brookhaven National Laboratory, UCB-88 in. is a cyclotron at Lawrence Berkeley Laboratories, Orsay is a new shut-down cyclotron at the Institut de Physique Nucleaire, Orsay, France.

Table 2. Recent JPL SEU Data (Bipolar Devices)

Device	Function	Technology	Mfr.	Bits	Threshold** Device Cross*** Cross Section		Facility	Remarks
					LET (MeV/mg/cm ²)	Section (cm ²) (Kr or Br)		
54L73 (new)	J/K Flip-Flop	L/TTL	T.I.	4	50	No upset	UCB-88 in	Date Code 8251
54L73 (old)	J/K Flip-Flop	L/TTL	T.I.	4	30	10 ⁻⁴	UCB-88 in	Vintage 1974
54L93 (new)	Counter	L/TTL	T.I.	4	30	-	BNL	Date code 8246
54L93 (old)	Counter	L/TTL	T.I.	4	12	4.5 x 10 ⁻⁴	BNL	Vintage 1974
93L422	RAM	L/TTL	AMD	1K	<3	4 x 10 ⁻²	UCB-88 in	Retest
AM6012	DAC	Bipolar	AMD	-	15	10 ⁻⁶	UCB-88 in	
AD562	DAC	Bipolar	AD	-	15	10 ⁻⁶	UCB-88 in	
AD573	A/D (10-bit)	Bipolar	AD	-	5	-	UCB-88 in	Part area > Beam area
MN5253	A/D (12-bit)	Bipolar	Micro- Networks	-	<<5	-	UCB-88 in	Part area > Beam area

TABLE 3. RECENT AEROSPACE SEU DATA (CMOS and Bipolar Devices)

Device	Function	Technology	Mfr.	Bits	Threshold LET (MeV/mg/cm ²)	Device Cross Section (K or Br)	Cross Section Per Bit (10 ⁻⁸ cm ²)	Facility	Remarks
ROC85	Microprocessor	CMOS/EPL	Harris		30			UCB 88-in.	5V, 10V Bias, respectively
SA3000	Microprocessor	CMOS/EPL	Sandila		30, 60	varies		UCB 88-in.	
TA13316	RAM	CMOS/SOS	RCA	16K	>80	No upset	0	UCB 88-in.	Multiple SEU's; Latchup
INI1600	RAM	NHOS	INMOS	64K	2	2	3125	UCB 88-in.	Latchup
INI1601	RAM	NHOS	INMOS	64K	<3	0.1	156	UCB 88-in.	Latchup
PACE422	RAM	Adv. CMOS	Perf. Semi.	1K	3	3 x 10 ⁻⁴	30	UCB 88-in.	
CM6167	RAM	CMOS/SOS	RCA	16K	15	4.6 x 10 ⁻⁴	3	UCB 88-in.	
HC6167R	RAM	CMOS/EPL	Honeywell	16K	>80	No upset	0	UCB 88-in.	
HS6504RRH	RAM	CMOS/EPL	Harris	4K	40	6.5 x 10 ⁻⁸	0	UCB 88-in.	Add. Latch error only
HS6526ZRRH	RAM	CMOS/EPL	Harris	16K	>80	No upset	0	UCB 88-in.	Variant of 93L422
AH9122	RAM	TTL	AMD	1K	2	4 x 10 ⁻²	4000	UCB 88-in.	
99C641	RAM	NHOS	AMD	64K	3	0.1	156	UCB 88-in.	
MDC5114	RAM	CMOS/SOS	Marconi	4K	50	7 x 10 ⁻⁴	16	UCB 88-in.	
HB81256	DRAM	NHOS	Fujitsu	256 K	2.5	~0.2		UCB 88-in.	Multiple upsets per strike
52833	EEPROM	NHOS	SEEQ	16K	2	2 x 10 ⁻⁴	1	UCB 88-in.	Write/erase errors only
54AHC1109	DUAL J/K FF	Adv. HCMOS	Zytex	2	60	10 ⁻⁶	50	UCB 88-in.	
54AHC1373	OCTAL LATCH	Adv. HCMOS	Zytex	8	28	2 x 10 ⁻⁵	250	UCB 88-in.	
54AHC1374	OCTAL D-FF	Adv. HCMOS	Zytex	8	28	4 x 10 ⁻⁵	500	UCB 88-in.	
54AS109	DUAL J/K FF	Adv. Schottky T.I.	T.I.	2	6	8 x 10 ⁻⁵	4000	UCB 88-in.	
54AS374	OCTAL D-FF	Adv. Schottky T.I.	T.I.	8	7	3 x 10 ⁻⁴	4000	UCB 88-in.	
54AS533	OCTAL D-LATCH	Adv. Schottky T.I.	T.I.	8	28	3 x 10 ⁻⁵	375	UCB 88-in.	
54HC165	SHIFT REG	HCMOS	T.I.					UCB 88-in.	Latchup (LET ~55)
54HC280	PARITY CHECKER	HCMOS	T.I.					UCB 88-in.	(2)
54HC373	OCTAL LATCH	HCMOS	RCA	8	40	4 x 10 ⁻⁶	40	UCB 88-in.	
54HC373	OCTAL LATCH	HCMOS	Supertex	8	80	No upset	0	UCB 88-in.	
54HC85	COMPARATOR	HCMOS	T.I.					UCB 88-in.	(2)
54HC100	AND GATE	HCMOS	RCA					UCB 88-in.	(1)
54HC104	HEX INVERTER	HCMOS	RCA					UCB 88-in.	(1)
54HC108	QUAD AND GATE	HCMOS	RCA					UCB 88-in.	(1)
54HC110	AND GATE	HCMOS	RCA					UCB 88-in.	(1)
54HC1109	DUAL J/K F/F	HCMOS	RCA					UCB 88-in.	(1)
54HC1138	DECODER	HCMOS	RCA					UCB 88-in.	(3)
54HC1163	COUNTER	HCMOS	RCA					UCB 88-in.	(3)
54HC1164	SHIFT REG.	HCMOS	RCA					UCB 88-in.	(3)
54HC1165	SHIFT REG.	HCMOS	RCA					UCB 88-in.	(3)
54HC1240	LINE DRIVER	HCMOS	RCA					UCB 88-in.	(1)
54HC1244	LINE DRIVER	HCMOS	RCA					UCB 88-in.	(1)
54HC1245	BUS TRANSCIEVER	HCMOS	RCA					UCB 88-in.	(1)
54HC127	MOR GATE	HCMOS	RCA					UCB 88-in.	(1)
54HC1374	OCTAL D-FF	HCMOS	RCA					UCB 88-in.	(1)
54HC1688	8-BIT COMPARATOR	HCMOS	RCA					UCB 88-in.	(1)
54HC174	DUAL D F/F	HCMOS	RCA					UCB 88-in.	(1)
54NC147	ENCODER	HCMOS	T.I.					UCB 88-in.	(1)
54NC160	COUNTER	HCMOS	T.I.					UCB 88-in.	(1)
54NC164	SHIFT REG.	HCMOS	T.I.					UCB 88-in.	(2)
54NC166	SHIFT REG.	HCMOS	T.I.					UCB 88-in.	(2)
54NC174	HEX D F/F	HCMOS	T.I.					UCB 88-in.	(2)
54NC273	OCTAL LATCH	HCMOS	T.I.					UCB 88-in.	(2)

- (1) Latchup test only at 90°C. No latchups observed with krypton.
 (2) Latchup test only at 25°C. No latchup observed with krypton at 60° angle.
 (3) Latchup test at 25°C and 90°C. No latchup observed with krypton at 60° angle.

LABORATORY OPERATIONS

The Aerospace Corporation functions as an "architect-engineer" for national security projects, specializing in advanced military space systems. Providing research support, the corporation's Laboratory Operations conducts experimental and theoretical investigations that focus on the application of scientific and technical advances to such systems. Vital to the success of these investigations is the technical staff's wide-ranging expertise and its ability to stay current with new developments. This expertise is enhanced by a research program aimed at dealing with the many problems associated with rapidly evolving space systems. Contributing their capabilities to the research effort are these individual laboratories:

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Chemistry and Physics Laboratory: Atmospheric chemical reactions, atmospheric optics, light scattering, state-specific chemical reactions and radiative signatures of missile plumes, sensor out-of-field-of-view rejection, applied laser spectroscopy, laser chemistry, laser optoelectronics, solar cell physics, battery electrochemistry, space vacuum and radiation effects on materials, lubrication and surface phenomena, thermionic emission, photo-sensitive materials and detectors, atomic frequency standards, and environmental chemistry.

Computer Science Laboratory: Program verification, program translation, performance-sensitive system design, distributed architectures for spaceborne computers, fault-tolerant computer systems, artificial intelligence, micro-electronics applications, communication protocols, and computer security.

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